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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,132	WON ET AL.	
	Examiner	Art Unit	
	JASON PROCTOR	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-3 are presented for examination.

Claims 1-3 are rejected.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 1 is objected to because of the following informalities: Claim 1 recites the parenthetical clause "(which will be referred to as an "tapered material layer") which needlessly interferes with interpreting the claim language. It is established US practice to refer to a claim element by using the specific phrase that describes the element. Appropriate correction is required.

3. Claim 2 is objected to because of the following informalities: Claim 2 recites the phrase "and/or" in line 8 which is interpreted as meaning "or". Applicants are requested to amend this phrase to recite "or", or alternatively to recite "and" if the Examiner's interpretation is not agreeable.

4. The Examiner respectfully submits that claims 1-3 are drafted in a way that makes claim interpretation challenging. In addition to the specific issues raised as claim objections or under 35 U.S.C. § 112, first and second paragraphs, the Examiner respectfully requests that Applicants consider drafting claims that recite a method which positively and directly recites the steps of the invention, as supported by the specification and the drawings.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-3 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claims are indefinite for several reasons as set forth below. As a result of that indefiniteness, it is unclear what Applicants are seeking to patent. It is unclear whether the invention is a computer simulation of an electronic device, a simulation of an electronic device manufacturing method, or an electronic device manufacturing method. The specification does not appear to overcome the deficiencies of the claim language. Therefore, the disclosure of the application, in light of the claim language, does not provide enabling disclosure. A person of ordinary skill in the art would be unable to make and/or use an invention where it is unclear to what field of technology the invention belongs.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-3 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. It is unclear from the claim language whether Applicants are claiming to have invented a computer simulation, a manufacturing method, or both. The claim language appears to alternate between a description of a computer simulation and a description of a manufacturing process (e.g. compare claim 1, "the three-dimensional structure is defined during the computer simulation" to claim 3, "filling a space between the upper substrate and the lower substrate with the intermediate insertion layer").

The claims are generally narrative because of the phrases "when" and "followed by" used throughout the claim language. These phrases vaguely imply a sequential order to the method. In order to comply with 35 U.S.C. § 112, second paragraph, the Examiner respectfully suggests that the method be drafted with sequentially labeled steps [e.g., A)…, B)…, C)…] and delete the narrative language.

7. Claim 1 recites "a method for defining a three-dimensional structure" and "wherein the three-dimensional structure is defined during the computer simulation" by a series of steps which appear to be integrated circuit manufacturing steps. The scope of this claim language is vague

and indefinite. Integrated circuit manufacturing steps of the type recited by the claim would be interpreted by a person of ordinary skill in the art as producing an electronic device on a substrate. These steps do not appear to "define a three-dimensional structure ... during computer simulation".

It is unclear whether Applicants are claiming:

1) a new simulation of a conventional method of manufacturing an electronic device on a substrate;

2) a new simulation of an electronic device on a substrate, wherein the device is described via the integrated circuit manufacturing steps used to create the real electronic device;

3) a conventional simulation of a new method of manufacturing an electronic device on a substrate; or

4) some other interpretation of the claim language.

The Examiner respectfully submits that **manufacturing a semiconductor** and **simulating a device and/or its manufacture** are regarded as **separate and distinct technologies** by the USPTO and are given **separate and distinct** classifications according to the US Patent Classification Manual. Therefore, it is critical that the claim language clearly delineate whether the invention is a **simulation** or a **method of manufacturing** an electronic device on a substrate.

8. Claim 2 recites steps of "designating," "designating," and "determining". These steps appear to be purely **abstract** and do not produce any tangible result. The scope of an abstract method is vague and indefinite. The scope of claim 2 is unknown.

9. Claim 3 recites several apparently optional steps. The scope of claim 3 is vague and indefinite.

Claim 3 recites several steps such as "c) **when** forming the material layer using a mask…" which are vague and indefinite. It is unclear whether this step would ever be performed during "a method for defining a three-dimensional structure".

Claim 3 recites steps such as "i) filling a space between the upper substrate and the lower substrate with the intermediate insertion layer" which appears to be an electronic device manufacturing step. It is unclear how this step is related to "a method of defining a three-dimensional structure … through computer simulation".

10. Claim 3 recites the limitation "the liquid crystal region" in step h). There is insufficient antecedent basis for this limitation in the claim.

Claim Interpretation

According to MPEP 2143.03, a claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. § 112, second paragraph, and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. However, it is improper to rely on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. § 103 on these assumptions).

In light of the specification, the invention is generally interpreted as a method of producing a computer simulation model of an electronic device. The electronic device is described in the claim language via the manufacturing steps that could be used to create a corresponding real electronic device. A substantial part of the claim language appears to describe the manufacturing steps, and therefore describe the computer simulation model only indirectly. The prior art renders this interpretation obvious as shown below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor

and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

11. Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Pregrant Publication 2003/0014146 to Fujii et al. ("Fujii") in view of "Reduced Process Method for Thin-Film-Transistor Liquid-Crystal-Display (TFT-LCD) with Dry-Etching Tapered ITO Data Bus Lines" by Yasuhiro Ugai et al. ("Ugai").

Regarding claim 1, Fujii teaches a method for defining a three-dimensional structure comprising a plurality of material layers between upper and lower substrates through computer simulation using input data of mask layout [*"The input unit 1 is a device inputting, for example, data regarding process conditions and data regarding mask conditions, and is implemented by, for example, a keyboard, a mouse, and/or a voice device. Input data to be input using the input unit 1 may include:* [...] *8) information regarding the mask pattern layout (i.e. mask pattern coordinates, measurements, layout, process conversion difference, process conversion coefficient);"* (Fujii, paragraphs 0028-0037)].

Fujii does not expressly teach the claimed three-dimensional structure.

Ugai teaches that the three-dimensional structure is defined by depositing material layers on the upper and lower substrates acting as reference base planes, respectively, and sandwiching an intermediate insertion layer between the upper and lower substrates with the material layers thereon facing each other, in particular, when at least one of the material layers has a tapered

region (which will be referred to as an "tapered material layer"), which is not parallel to the upper and lower substrates and is inclined to the base planes [*"For years, many studies have been conducted for the purpose of reducing the number of TFT processes. We have developed a top-gate TFT-LCD fabricated using only indium-tin-oxide (ITO: In_2O_3-SnO_2) data bus lines by eliminating the metal data bus line process. Substituting ITO dry-etching for wet-etching allows tapering of the side walls of thick ITO data bus lines. Controlling the tapered angle of ITO data bus lines to be less than 40° results in successful fabrication of a transistor with no offset voltage. As a result, we have developed a 6-inch-diagonal TFT-LCD fabricated with data bus lines as well as drain-source electrodes of a single-layered ITO."* (Ugai, abstract); *"As shown in Fig. 2, a metal film was generally applied in the case of the conventional TFT in order to lower the resistance of data bus lines without increasing the ITO thickness."* (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); *"The fabrication process of the top-gate TFT used in this work is shown in Fig. 6. After the ITO drain-source and bus lines are patterned, phosphorus (P) deposition is carried out by exposing the substrate to a radio frequency (RF: 13.56 MHz) glow discharge of phosphine (PH_3) while maintaining the temperature at 250℃. P treatment conditions are as follows: substrate temperature = 250℃, PH_3 flow (0.5% in Ar) = 1500 sccm, RF power = 100W, pressure = 40 Pa, ITO data bus line thickness = 150nm."* (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)].

Fujii and Ugai are analogous art because both are drawn to the manufacture of electronic devices.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Fujii and Ugai as expressly motivated by Ugai to manufacture a TFT panel using a process *"which achieves lower production cost as a result of a reduction in the number of TFT processes"* (Ugai, page 1027, left column). The combination of the prior art teachings could be achieved by using the parameters and other information taught by Ugai (e.g., Ugai, page 1028, "3. Procedure of Top-Gate TFT Fabrication") as input data for the computer simulation method taught by Fujii (especially Fujii, paragraphs 0028-0037). As a result, Fujii teaches that *"The input data processing unit 11 of the CPU 5 is a processing unit that automatically converts input data into, for example, formatted data for desired simulation or formatted data for the critical condition storage unit 6... In addition, the universal simulation unit 12 encompasses a single simulator connected thereto, which performs calculation using the finite element method, boundary element method, difference methods, or molecular dynamics. Here the universal simulation unit 12 may freely set which simulator is to be used for each process..."* (Fujii, paragraph 0039) and *"The display unit 2 is a device for showing, for example, processing results from simulation, locations where input data is to be corrected, and reasons for defects (NG)"* (Fujii, paragraph 0038). Therefore, by using Ugai's teachings for manufacturing a TFT-LCD as input data for Fujii's simulation and display, a person of ordinary skill in the art would arrive at the invention specified in claim 1.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Fujii and Ugai to arrive at the invention specified in claim 1.

Regarding claim 2, Fujii in view of Ugai teaches the method as set forth in claim 1, comprising the steps of:

a) designating a certain material layer as the intermediate insertion layer among the plurality of material layers formed between the upper and lower substrates, followed by designating parameters including a thickness of the intermediate insertion layer and/or a kind of material thereof [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

b) designating information of a name, a kind of material, a thickness, and an associated mask for each of the plurality of material layers deposited onto the upper substrate and the lower substrate formed at upper and lower surfaces of the three-dimensional structure with the intermediate insertion layer formed at the center between the upper and lower substrates, and information of a taper angle of the tapered material layer when the at least one of the material layers has the tapered region, which is not parallel to the upper and lower substrates and is inclined to the base planes, followed by defining a deposition sequence for the material layers on the upper and lower substrates, respectively [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037); and

c) determining whether each of the material layers is formed by use of polygons defining a mask layout object defined for the associated mask as a lower surface of the material layer or by use of remaining regions as the lower surface of the material layer except for the polygons

defining the mask layout object defined for the associated mask [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037).

Regarding claim 3, Fujii in view of Ugai teaches the method as set forth in claim 1, comprising the steps of:

a) forming an internal polygon within a polygon defining a mask layout object for a mask having a designated taper angle, the internal polygon having a size smaller than the polygon defining the mask layout object while having the same shape and sequence of apexes as those of the polygon defining the mask layout object, followed by forming side polygons dividing a planar space between the internal polygon and the polygon defining the mask layout object by connecting the apexes of the internal polygon to the associated apexes of the polygon defining the mask layout object such that the apexes having the same sequences are connected to each other from the internal polygon to the polygon defining the mask layout object [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

b) forming lines at both sides of edges of each of polygons defining a mask layout object defined for another mask except for the mask having the designated taper angle so as to be parallel to both sides of the edges of each of the polygons at an overlap region between the polygons defining the mask layout object defined for the other mask except for the mask having

the designated taper angle and the polygon defined for the mask having the designated taper angle, followed by dividing the polygon defined for the mask having the designated taper angle by use of the lines [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

c) when forming the material layer using a mask without the designated taper angle or the material layer formed without a designated mask according to information of a deposition sequence for the material layers on the lower substrate, depositing a material for the material layer using the mask without the designated taper angle to have a thickness designated by a user upward from an upper surface of the material layer previously defined on the lower substrate [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

d) when forming the material layer using the mask having the designated taper angle according to the information of the deposition sequence of the material layers on the lower substrate, defining the mask layout object as a lower surface of the material layer using the mask having the designated taper angle over the upper surface of the material layer previously defined on the lower substrate, the internal polygon of the mask layout object as an upper surface of the material layer using the mask having the designated taper angle at a position spaced a predetermined thickness from the upper surface of the material layer previously defined on the lower substrate, and the side polygons of the mask layout object as side surface of the material layer using the mask having the designated taper angle, respectively, followed by depositing a

new material for the material layer formed using the mask having the designated taper angle in a region surrounded by the polygon of the lower surface, the polygon of the upper surface, and the polygons of the side surfaces [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

e) when forming the material layer using the mask without the designated taper angle or the material layer formed without using the designated mask according to the information of the deposition sequence of the material layers on the upper substrate, depositing another new material for the material layer formed using the mask without the designated taper angle or the material layer formed without using the designated mask to have a predetermined thickness downward from a lower surface of the material layer previously defined on the upper substrate [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

f) when forming the material layer using the mask having the designated taper angle according to information of a deposition sequence of the material layers on the upper substrate, defining the mask layout object as an upper surface of the material layer using the mask having the designated taper angle over the lower surface of the material layer previously defined on the upper substrate, the internal polygon of the mask layout object as a lower surface of the material layer using the mask having the designated taper angle at a position spaced a predetermined thickness downward from the lower surface of the material layer previously defined on the upper substrate, and the side polygons of the mask layout object as side surfaces of the material layer

using the mask having the designated taper angle, respectively, followed by depositing another new material for the material layer formed using the mask having the designated taper angle in a region surrounded by the polygon of the upper surface, the polygon of the lower surface, and the side surfaces [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

g) when forming the material layer using the mask having the designated taper angle according to the information of the deposition sequence of the material layers on the upper substrate, depositing another new material for the material layer downwardly, the material layer using the mask layout object as an upper surface of the material layer using the mask having the designated taper angle on the lower surface of the material layer previously defined on the upper substrate, the internal polygon of the mask layout object as a lower surface of the material layer using the mask having the designated taper angle at a position spaced the predetermined thickness downward from the lower surface of the material layer previously defined on the upper substrate, and the side polygons of the mask layout object as side surfaces of the material layer using the mask having the designated taper angle [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037);

h) displacing the upper substrate upward such that the highest apex among the apexes of the polygons constituting the upper surface of the defined lower substrate is located at a position spaced a thickness of the crystal liquid region designated by the user from the lowest apex

among the apexes of the polygons constituting the upper surface of the defined lower substrate [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037); and

i) filling a space between the upper substrate and the lower substrate with the intermediate insertion layer [(Ugai, abstract); (Ugai, page 1027, left column); (Ugai, page 1027, Fig. 2); (Ugai, page 1027, Fig. 3); (Ugai, page 1028, right column, "3. Procedure of Top-Gate TFT Fabrication"); (Ugai, page 1029, Fig. 6)] See also (Fujii, paragraphs 0028-0037).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jason Proctor/
Examiner
Art Unit 2123

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